THAT WHICH IS CLAIMED IS:

1. Process for characterization of a CMOS logical cell for manufacturing in partially depleted silicon-on-insulation technology, comprising modeling the cell, and a phase for determining internal potentials of the cell based on functional simulation of the modeled cell utilizing a binary stimulation signal (ST) and in which the floating substrate (B) of each transistor and the cell, and at predetermined successive instants of injection, is injected with a charge proportional to the variation of the internal potential of this transistor, a variation determined during a predetermined time interval (TC) of the stimulation signal preceding the current instant of injection and exempt from injection,

2. Process as claimed in Claim 1, characterized in that an injection current corresponding to the injected charge is determined such that after injection the variation of the internal potential (Vb) of the transistor in question reaches n times said measured variation of the internal potential,

3. Process as claimed in Claim 2, characterized in that the value of n is determined from measuring the variation of the internal potential of a transistor of the cell, during a cycle of the stimulation signal. and from the estimated amplitude of the variation of the internal potential of this transistor between its state of static equilibrium and its state of dynamic equilibrium.

4. Process as claimed in one of the foregoing claims, characterized in that the value of the proportionality coefficient (A) is determined from measuring the variation of the internal potential and from the charge variation of a transistor of the cell during a cycle of the stimulation signal, and of the duration of injection.

5. Process as claimed in one of the foregoing claims, characterized in that the stimulation signal (ST) comprises in each period a transition separating two plateau, in that an injection instant is located during a plateau and at a transition distance, and in that the duration of injection of the current is selected greater than the time pitch of the functional simulation and less than the duration of a plateau.

6. Process as claimed in one of the foregoing claims, characterized in that consecutive injection instants are spaced at an interval equal to two periods of the stimulation signal, and in that said time interval (TC) has a duration equal to a period of the stimulation signal.

7. Process as claimed in Claim 6, characterized in that the initial instant (t0) of the time interval precedes the injection instant of 1.5 periods of the stimulation signal, and the final instant (tf) of the time interval precedes the injection instant of 0.5 period of the stimulation signal.

8. Process as claimed in one of the foregoing claims, characterized in that for functional simulation

each transistor of the cell is replaced by a model of this transistor linked to three voltage-controlled modeled voltage sources, enabling an internal potential target (Vbc) of the transistor to be reached to be determined after injection, and to a modeled current source supplying an injection current proportional to the difference between the internal potential target and the internal potential at the injection instant.

9. Process as claimed in Claims 7 and 8, characterized in that the first voltage source supplies at the injection instant the value of the internal potential of the transistor delayed by a period of the stimulation signal, in that the second voltage source supplies the variation of the internal potential over a period, delayed by a half period of the stimulation signal, and in that the third voltage source supplies the internal potential target (Vbc).

10. Process as claimed in one of the foregoing claims, characterized in that the evolution of the internal potentials of the transistors of the cell are determined from the state of static equilibrium to the state of dynamic equilibrium, relative to the rising and falling transitions of the stimulation signal and for the two initial values of the stimulation signal, and in that the internal potentials of the transistors corresponding to the worst case or the best case of time delay of the cell are deduced therefrom.

11. Process as claimed in one of the foregoing claims, characterized in that it comprises determining the evolution of the different time delays

of the cell, as well as determining time delays corresponding to the worst case or best case scenario.

12. Process as claimed in one of the foregoing claims, characterized in that the evolution of other parameters for characterizing the cell is determined, as well as the values of these parameters corresponding to the worst case or the best case scenario.

13. Device for characterizing a CMOS logical cell for manufacturing in partially depleted silicon-on-insulation technology, comprising modeling means (MDL) of the cell and processing means (MT) suitable for effecting a determination phase of the internal potentials of the cell based on functional simulation of the modeled cell using a periodic binary stimulation signal and in which the processing means are suitable for injecting the floating substrate of each transistor of the cell, and at predetermined successive instants of injection, with a charge proportional to the variation of the internal potential of this transistor determined during a predetermined time interval of a stimulation signal preceding the current injection instant and exempt from injection, so as to accelerate the charge or discharge of the floating substrate of the transistor.

14. Device as claimed in Claim 13, characterized in that the processing means (MT) determine an injection current corresponding to the injected charge such that after injection the variation of the internal potential of the transistor in question reaches n times said measured variation of the internal

potential.

15. Device as claimed in Claim 14, characterized in that the processing means (MT) determine the value of n from measuring the variation of the internal potential of a transistor of the cell in a cycle of the stimulation signal and from an estimated amplitude of the variation of the internal potential of this transistor between its state of static equilibrium and its state of dynamic equilibrium.

16. Device as claimed in one of Claims 13 to 15, characterized in that the processing means determine the proportionality coefficient (A) from measuring the variation of the internal potential and from the charge variation of the transistor of the cell during a cycle of the stimulation signal, and of the injection duration.

17. Device as claimed in one of Claims 13 to 16, characterized in that the stimulation signal (ST) comprises in each period a transition separating two plateau, in tat an injection instant takes place during a plateau at a transition distance, and in that the duration of injection of the current is selected greater than the time pitch of the functional simulation and less than the duration of a plateau.

18. Device as claimed in one of Claims 13 to 17, characterized in that two consecutive injection instants spaced by a period equal to two periods of the stimulation signal, and in that said time interval has duration equal to a period of the stimulation signal.

19. Device as claimed in Claim 18, characterized in that the initial instant of the time interval precedes the injection instant by 1.5 periods of the stimulation signal, at the final instant of the time interval precedes the instant of injection by 0.5 period of the stimulation signal.

20. Device as claimed in one of Claims 13 to 19, characterized in that the modeling means (MDL) comprising for each transistor of the cell a half of this transistor linked to three modeled voltage-controlled voltage sources, allowing an internal potential target of the transistor to be attained after injection to be determined, and to a modeled current source supplying an injection current proportional to difference between the internal potential target and the internal potential at the instant of injection.

21. Device as claimed in Claims 19 and 20, characterized in that the first voltage source supplies the injection instant, the value of the internal potential of the transistor delayed by a period of the stimulation signal, in that the second voltage source supplies the variation of the internal potential over a period, delayed by a period of the stimulation signal, and in that the third voltage source supplies the internal potential target.

22. Device as claimed in one of Claims 13 to 21, characterized in that the processing means are suitable for determining the evolution of the internal potentials of the transistors of the cell from the state of static equilibrium to the state of dynamic equilibrium, relative to the rising and falling

transitions of the stimulation signal and for the two initial values of the stimulation signal, and for deducing the internal potentials of the transistors corresponding to the worst-case or the best-case scenario.

23. Device as claimed in Claim 22, characterized in that the processing means are suitable for determining the evolution of different time delays of the cell, and for determining the time delays corresponding to the worst-case or the best-case scenario.

24. Device as claimed in Claim 23, characterized in that the processing means are suitable for determining the evolution of other acceleration parameters of the cell and for determining the values of these parameters for the worst-case or the best-case scenario.